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PATENT ABSTRACTS OF JAPAN

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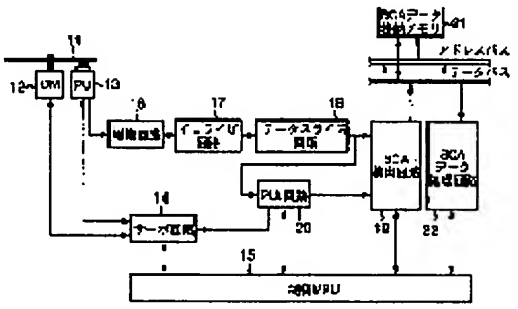
(54) DATA-REPRODUCING APPARATUS

(57)Abstract:
PROBLEM TO BE SOLVED: To fix the data length and facilitate the processing of data strings by generating an address to be fed to a recording medium from a synchronous code and a frame number in a reproduced data packet, and recording data of the reproduced data packet on the basis of the address on the recording medium.
SOLUTION: A BCA detection circuit 19 deletes a line sending a recording length to a BCA data-processing circuit 22 therefrom without detecting the recording length of BCA data. In detecting the BCA data, a control MPU generates a memory initialization instruction to a memory initialization control circuit of the BCA detection circuit 19 via an input terminal. The BCA data having a not specified data length are fixed in data length by initializing contents in a BCA data-storing memory 21. Accordingly, an ECC operation process and an EDC operation process can be carried out uniformly with a process of a maximum data length irrespective of the data length of the BCA data, thereby eliminating detection of the recording length of the BCA data.



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CLAIMS

[Claim(s)]
[Claim 1]A data reproduction apparatus which reproduces a data row which one data packet comprises a frame of an unspecified number, and comprises data of a predetermined number in which one frame was given a synchronization code and a frame number, respectively, comprising:
A recording medium which has the storage capacity which can record said one data packet in which a frame of the maximum number was contained.
An initializing means which records and initializes specific data to a record section for said one data packet of this recording medium.
A recording device which generates an address given to said recording medium from said synchronization code and a frame number which are contained in a reproduced data packet, and records data of said reproduced data packet on said recording medium based on this generated address.

[Claim 2]The data reproduction apparatus according to claim 1, wherein said specific data is zero data.
[Claim 3]The data reproduction apparatus according to claim 2 using as un-0 data said specific data recorded on a field corresponding to a head frame and a final frame of said one data packet in said recording medium.
[Claim 4]The data reproduction apparatus according to claim 1, wherein said data row is BCA data.
[Claim 5]The data reproduction apparatus according to claim 1 generating identification information which shows whether said recording device recorded data of said reproduced data packet on said recording medium.
[Claim 6]The data reproduction apparatus according to claim 5 which possesses a means to process a data packet recorded on said recording medium, based on said identification information, and is characterized by things.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to improvement of the data reproduction apparatus which reproduces the data whose data length is un-specific.
[0002]
[Description of the Prior Art]As everyone knows, recently, DVD (Digital Video Disk) is developed as an optical disc which recorded a vast quantity of abbreviation 5G bit data on one side, and the DVD reproducer which plays this DVD is also spreading through a commercial scene.
[0003]By the way, after a manufacturing process is completed, for example at a factory etc. to this DVD, as shown in drawing 4, the so-called BCA (Burst Cutting Area) code may be further recorded on the specific region of inner circumference by the YAG laser rather than that read in area.
[0004]Drawing 5 shows the structure of one packet of such BCA data. The number of BCA user data has 16n-four (1<=n<=12) bytes' variable information area, and to this First, 4 bytes of EDC (Error Detection Code) parity, 16 bytes of ECC (Error Correction Code) parity is added.
[0005]And 1 byte of sync data RSBCAn are added to this variable information area and EDC parity every 4 bytes, respectively, and 1 byte of sync-data RSBCA13 is added to them every 4 bytes at ECC parity.
[0006]As for this BCA data, 1 byte of sync data SBBCA and 4 bytes of BCA-Preamble data whose each is "00h (Hexa-decimal)" are added to that head part.
[0007]After that ECC parity, 1 byte of sync-data RSBCA14 and 4 bytes of BCA-Postamble data whose each is "55h" are added, and, as for this BCA data, 1 byte of sync-data RSBCA15 is added after that.
[0008]And each sync data SBBCA and RSBCAn, RSBCA13, RSBCA14, and RSBCA15 comprise 8 channel bits which express a specific sink pattern, respectively, and 8 channel bits showing frame number n. 1 bit follows the modulation rule which becomes two channel bits.
[0009]Here, although the number of user data of one frame is formed at 16 bytes, only the n-th frame, the number of user data will be 12 bytes, and 4 bytes of EDC parity is added. For example, if it becomes n=5, the number of user data will be 16x5-4=76 byte, and 4 bytes of EDC parity will be added after sync-data RSBCAof five frames5 of the 4th line.
[0010]16 bytes of reed-solomon ECC parity which interleave processing is carried out and is added to the lengthwise direction of this BCA data structure belongs to 13 frames irrespective of user-datum length. For example, if it becomes n=5, sync-data RSBCA13 will appear after the EDC parity of five frames, and ECC parity will continue.
[0011]As mentioned above, rather than read in area of DVD, it has still more sufficient width on the concentric circle of inner circumference, and this BCA data is recorded, and its data non-record section in the BCA data recording regions on DVD increases, so that data length is short.
[0012]And the modulation rule of this BCA data is assigning two channel bits of "10" and "01" to

the 1-bit data showing "0" and "1", respectively. A specific sink pattern is "01000110" from a higher rank, and the frame number following this is modulating the 4-bit data showing "0"- "13" to eight channel bits in accordance with the modulation rule mentioned above.
[0013]If this modulation rule is followed, the minimum polarity-reversals interval Tmin of data will be set to 1T, the maximum polarity-reversals interval Tmax will be set to 4T, and this 4T pattern will appear only in sync data.
[0014]Drawing 6 shows the refreshable disk reproduction device for the optical disc in which such BCA data was recorded. In drawing 6, the numerals 11 are the optical discs in which BCA data was recorded, and are rotated with the disk motor 12. The signal recording surface of the optical disc 11 is countered, and the optical pick-up 13 is installed.
[0015]As for this disk motor 12, that revolving speed is controlled by the servo circuit 14. While a tracking servo and a focus servo are given, movement to the diameter direction of the optical disc 11 is controlled. [as opposed to / in the optical pick-up 13 / the object lens which is not illustrated by the servo circuit 14]
[0016]When playing the BCA data of the optical disc 11, control MPU(Micro-Processing Unit) 15 which controls operation of a disk reproduction device in generalization here, While giving a CAV (Constant Angular Velocity) servo by the servo circuit 14 so that the optical disc 11 may be kept at 24 Hz (1440 rpm) which is the optimal number of rotations for playback of BCA data, The optical pick-up 13 is moved to the record section of BCA data.
[0017]And after passing the amplifying circuit 16 and the equalizer circuit 17, the electrical signal corresponding to the BCA data outputted from the optical pick-up 13 is supplied to the data slicing circuit 18, and is binary-ized. This binary-ized signal is supplied to the BCA detector circuit 19 and the PLL (Phase Locked Loop) circuit 20.
[0018]Among these, PLL circuit 20 generates a channel bit clock from the inputted binary-ized signal, and is outputting it to the BCA detector circuit 19. From the inputted binary-ized signal, the BCA detector circuit 19 samples data based on a channel bit clock, and is generating the BCA detection channel bit.
[0019]And in this BCA detector circuit 19, the frame number has been obtained by detecting a sink pattern out of a BCA data stream, and restoring to the data of eight channel bits which continue after that based on a channel bit clock and a BCA detection channel bit.
[0020]Then, this BCA detector circuit 19 generates the row numbers in a frame from 0 to 3 to the obtained frame number, determines the address to the BCA data storage memory 21, and makes the BCA data to which it restored memorize one by one. 208 bytes is recorded, when this BCA data storage memory 21 is n= 12 when BCA data is the longest that is,.
[0021]As for the BCA data recorded on this BCA data storage memory 21, error detection based on [again] EDC parity in the error correction processing based on ECC parity is performed by the BCA data processing circuit 22.
[0022]Drawing 7 shows the details of the above-mentioned BCA detector circuit 19. That is, it is supplied to the sink detector circuit 19e while it is outputted to a data bus via the demodulator circuit 19b and the output terminal 19c, after the BCA binary-ized signal outputted from the above-mentioned data slicing circuit 18 passes the input terminal 19a. The channel bit clock outputted is supplied to the above-mentioned demodulator circuit 19b and the sink detector circuit 19e via the input terminal 19d from above-mentioned PLL circuit 20.
[0023]And the output of the above-mentioned demodulator circuit 19b and the output of the sink detector circuit 19e are outputted to the BCA data processing circuit 22 via 19h of BCA recording length detector circuits, and the output terminal 19i while they are outputted to an address bus via 19f of memory address generating circuits, and the output terminal 19g.
[0024]Here, if the above-mentioned optical pick-up 13 arrives at BCA data recording regions from the data non-record section of the optical disc 11, the channel bit which begins from the sync data SBBCA will be detected. Then, PLL circuit 20 locks and a regular channel bit clock comes to be

obtained in the hit which reproduces these sync data SBBCA and BCA-Preamble data.
[0025]At this time, first, the sink pattern of sync-data RSBCA1 is detected and the address 0 is generated in the BCA data storage memory 21 in the above-mentioned BCA detector circuit 19. Then, the BCA detector circuit 19 performs data demodulation processing which is detected and which makes it 1 byte every 16 channel bits, and is **********ing the address each time.
[0026]Thus, when the data for 4 bytes was recorded on the BCA data storage memory 21 next, sync-data RSBCA1 should be detected again, but. Even if undetectable, it continues without changing a data demodulation interval and increment of an address as what has detected sync data in false, and the BCA detector circuit 19 is performing what is called synchronous protection.
[0027]If the BCA detector circuit 19 sets up the sink detection window about **2 channel-bit width and sync data are detectable in this window to the predicted position which detects sync data, it will perform that position amendment and will correct subsequent data demodulation synchronizations.
[0028]When the sync data detected at this time are the values of RSBCA10 other than RSBCA1 (for example, RSBCA2), etc., the BCA detector circuit 19 considers that it is a detection error, and is kept from changing an address.
[0029]And when the demodulated data for 16 bytes is recorded on the BCA data storage memory 21, the sync data by which it is generated next must be RSBCA2 or RSBCA13, but. The BCA detector circuit 19 is not based on a frame number, but makes increment of an address continue, and is made to continue without also changing a data demodulation synchronization.
[0030]That is, even if there is a change data demodulation synchronous [by position amendment of **2 channel bit by sync data], increment is continued about an address. Thus, the address to each byte of the user datum, its EDC parity, and ECC parity at the time of generating an address will be generated as shown in drawing 8.
[0031]A recovery and record of data are performed by the above procedure, and recording operation is ended when 16 bytes of data in which sync-data RSBCA13 was added is recorded. Next, processing of an error correction, EDC error detection, etc. is performed to the data recorded on the above-mentioned BCA data storage memory 21 by the BCA data processing circuit 22. That is, in the above-mentioned BCA detector circuit 19, when recording BCA data on the BCA data storage memory 21, the recording address of final data (RSBCA13) was held and this address is sent out to the BCA data processing circuit 22.
[0032]In this BCA data processing circuit 22, first, although error correction processing by ECC parity is performed, ECC parity is generated by the syndrome calculation by the data permutation of a lengthwise direction here. Therefore, in this error correction processing, it is made to advance an address to a lengthwise direction by four rows.
[0033]Namely, since the ECC parity to which the data which is 16 bytes to which sync-data RSBCA3 was given per 4 bytes, next sync-data RSBCA13 were given continues in being n= 3, for example, From 0 to 15 becomes data of RSBCA1, from 16 to 31 becomes data of RSBCA2, from 32 to 47 becomes data of RSBCA3, and, as for an address, even 63 becomes the ECC parity of RSBCA13 from 48.
[0034]For this reason, the address generated for the error correction of the 1st row is 0->4->8->12->.... It is set to ->56 ->60 and ECC parity will exist in the position of the addresses 48, 52, 56, and 60. At the time of the error correction of the 2nd row, it is an address 1->5->9->13-> .... It is made to generate with ->57 ->61 and the addresses 49, 53, 57, and 61 serve as a position of ECC parity in this case.
[0035]Similarly, at the time of the error correction of the 3rd row, it is an address 2->6->10->14-> .... It is made to generate with ->58 ->62, In this case, the addresses 50, 54, 58, and 62 serve as a position of ECC parity, and it is an address at the time of the error correction of the 4th row 3->7->11->15-> .... It is made to generate with ->59 ->63 and the addresses 51, 55, 59, and 63 serve as a position of ECC parity in this case.

[0036]By the way, ECC parity is made from the format of the BCA code corresponding to the time of the maximum record length of a BCA user datum, i.e., the case of n= 12. For this reason, in the case of n!=12, zero data "00h" must be put into the crevice from EDC parity to ECC parity, and syndrome calculation must be performed.
[0037]For this reason, it is necessary to insert zero data "00h" in this crevice virtually, and to perform syndrome calculation also in the case of error correction processing of BCA data. If it says in the above-mentioned example (n= 3), in the case of the error correction of the 1st row. x (12-3) 4= 36 bytes of zero data "00h" needs to be inserted as a crevice at the time of the maximum record length between the address 44 in which EDC parity is located, and the address 48 in which the 1st byte of ECC parity is located.
[0038]And in the above-mentioned BCA data processing circuit 22. A crevice is calculated from the recording address of the recording length detected in 19 h of BCA recording length detector circuits of the BCA detector circuit 19, i.e., the data of sync-data RSBCA13 obtained by the above-mentioned record method, and zero dummy data "00h" is inserted.
[0039]That is, if it is n= 6, as for the 1st row, an address is 0->4->8->12->.... Since it is generated with ->104 ->108 and the address 96,100,104,108 serves as ECC parity in this case, Among the addresses 92 and 96, x (12-6) 4= 24 bytes of zero data "00h" will be inserted.
[0040]Next, data processing for the EDC error detection in the above-mentioned BCA data processing circuit 22 is explained. That is, he is trying to double processing with recording length using the recording address of the final data held at the time of data recording at the time of this EDC data processing as well as the time of ECC processing.
[0041]For example, if it is n= 3, the address generated will be 0 to 63 and the address of EDC parity will become 44, 45, 46, and 47 before long. For this reason, the address generated at the time of EDC data processing begins from 0, and is ended by 47. If it is n= 6, the address generated will be 0 to 111 and the address of EDC parity will become 92, 93, 94, and 95 before long. For this reason, the address generated at the time of EDC data processing begins from 0, and is ended by 95.
[0042]As mentioned above, BCA data in a refreshable disk reproduction device. For the error correction by ECC parity, or EDC check processing, supply the recording length whom the BCA detector circuit 19 detected to the BCA data processing circuit 22, and in the BCA data processing circuit 22. According to this inputted detection recording length, he chooses ECC-error-correction processing or EDC data processing, and is trying to change processing.
[0043]
[Problem(s) to be Solved by the Invention]However, in the above conventional disk reproduction devices. Since it has changed so that the recording length of BCA data may be detected and processing of ECC and EDC may be made to correspond according to this recording length that detected, the problem of the processing which BCA data reproduction takes being complicated, and circuitry being also complicated and enlarging it according to this has arisen.
[0044]Then, this invention was made in consideration of the above-mentioned situation, and does not need complicated processing which detects the recording length of BCA data, but it aims at providing the very good data reproduction apparatus which made it possible to process BCA data easily with simple composition.
[0045]
[Means for Solving the Problem]One data packet comprises a frame of an unspecified number, and a data reproduction apparatus concerning this invention is aimed at what reproduces a data row which comprises data of a predetermined number to which a synchronization code and a frame number were given, respectively by one frame.
[0046]And a recording medium which has the storage capacity which can record one data packet in which a frame of the maximum number was contained, An initializing means which records and initializes specific data to a record section for one data packet of this recording medium, An address given to a recording medium from a synchronization code and a frame number which are contained

in a reproduced data packet is generated, and it has a recording device which records data of a data packet reproduced based on this generated address on a recording medium.
[0047]When a frame number records an unspecified data row on a recording medium according to the above composition, Record specific data on a recording medium, initialize the contents, and an address given to a recording medium from a synchronization code and a frame number which are contained in a data packet reproduced on it is generated, Itis [fixed-length-] made toize data length by recording data of a data packet reproduced based on this generated address on a recording medium.
[0048]For this reason, as opposed to data of a data packet recorded on a recording medium irrespective of data length, can unify ECC data processing, EDC data processing, etc. into processing at the time of the maximum data length, can perform them now, and like before, It becomes possible to process a data row easily with simple composition, without needing complicated processing which detects recording length of BCA data.
[0049]
[Embodiment of the Invention]Hereafter, this embodiment of the invention is described in detail with reference to drawings. In drawing 1, identical codes are attached and shown in drawing 6 and identical parts. That is, it does not carry out detecting the recording length of BCA data in said BCA detector circuit 19, but the line which sends out recording length to the BCA data processing circuit 22 is deleted from the BCA detector circuit 19. And it has composition as shows drawing 2 the BCA detector circuit 19. In drawing 2, identical codes are attached and shown in drawing 7 and identical parts.
[0050]Here, said BCA data storage memory 21 has the capacity which can memorize 208 bytes which is a data number in case BCA data is the longest, i.e., n= 12. And in detecting BCA data, said control MPU15 generates memory initialization instructions via the input terminal 19j in the memory initialization control circuit 19k of the BCA detector circuit 19.
[0051]In response to these memory initialization instructions, the BCA detector circuit 19, To the BCA data storage memory 21, as shown in drawing 3, "FFh" is written in the addresses 0-15 as un-0 data, Memory initialization processing in which write zero data "00h" in the addresses 16-191, and "FFh" is written in the addresses 192-207 as un-0 data is performed.
[0052]This memory initialization processing by decoding the address generated in 19 f of memory address generating circuits by 19 l. of address decoders, By the addresses 0-15, and 192-207, so that un-0 data "FFh" may be generated from the output terminal 19c, The control signal A ("H"active) is outputted to 19 m of OR circuits, and in other addresses (16-191 are included), the control signal B ("L"active) is outputted to 19 n of AND circuits so that zero data "00h" may be generated from the output terminal 19c.
[0053]And when this memory initialization processing is completed, the BCA detector circuit 19 starts the detecting operation of BCA data. That is, control MPU15 generates instructions so that the optical pick-up 13 may be moved to the record section of BCA data, while making a CAV servo perform to the servo circuit 14 so that the optical disc 11 may be maintained at the optimal number of rotations for playback of BCA data.
[0054]Here, if the above-mentioned optical pick-up 13 arrives at BCA data recording regions from the data non-record section of the optical disc 11, the channel bit which begins from the sync data SBBCA will be detected. Then, PLL circuit 20 locks and a regular channel bit clock comes to be obtained in the hit which reproduces these sync data SBBCA and BCA-Preamble data.
[0055]At this time, first, the sink pattern of sync-data RSBCA1 is detected and the address 0 is generated in the BCA data storage memory 21 in the above-mentioned BCA detector circuit 19. Then, the BCA detector circuit 19 performs data demodulation processing which is detected and which makes it 1 byte every 16 channel bits, and is **********ing the address each time.
[0056]Thus, when the data for 4 bytes was recorded on the BCA data storage memory 21 next, sync-data RSBCA1 should be detected again, but. Even if undetectable, it continues without

changing a data demodulation interval and increment of an address as what has detected sync data in false, and the BCA detector circuit 19 is performing what is called synchronous protection.
[0057]If the BCA detector circuit 19 sets up the sink detection window about **2 channel-bit width and sync data are detectable in this window to the predicted position which detects sync data, it will perform that position amendment and will correct subsequent data demodulation synchronizations.
[0058]When the sync data detected at this time are the values of RSBCA10 other than RSBCA1 (for example, RSBCA2), etc., the BCA detector circuit 19 considers that it is a detection error, and is kept from changing an address.
[0059]And when the demodulated data for 16 bytes is recorded on the BCA data storage memory 21, the sync data by which it is generated next must be RSBCA2 or RSBCA13, but if the detected frame number is except 13, an address will continue increment, without changing.
[0060]When the sink pattern of sync-data RSBCA13 is detected in the window of **2 channel-bit width to a predicted position, 19 f of memory address generating circuits output the address 192 (address jump). Since this address 192 is equivalent to the address which writes in the 1st byte of RSBCA13 at the time of the maximum record length, zero data "00h" written in at the time of memory initialization will remain in the jumped addresses 16-191 after all. And recording operation is ended when 16 bytes of data in which sync-data RSBCA13 was added is recorded.
[0061]Next, processing of an error correction, EDC error detection, etc. is performed to the data recorded on the BCA data storage memory 21 as mentioned above by the BCA data processing circuit 22. First, address generation for the error correction processing by ECC parity is performed as follows.
[0062]That is, the address generated for error correction processing of the 1st row is 0->4->8->12->.... It is set to ->200 ->204 and ECC parity will exist in the position of the address 192,196,200,204. The address generated for error correction processing of the 2nd row is 1->5->9->13->.... It is set to ->201 ->205 and ECC parity will exist in the position of the address 193,197,201,205.
[0063]Similarly, the address generated for error correction processing of the 3rd row is 2->6->10->14->.... It is set to ->202 ->206 and ECC parity will exist in the position of the address 194,198,202,206. The address generated for error correction processing of the 4th row is 3->7->11->15->.... It is set to ->203 ->207 and ECC parity will exist in the position of the address 195,199,203,207.
[0064]And the ECC parity following sync-data RSBCA13 is recorded on the fixed position 192-207 of the memory 21, i.e., addresses, at the time of record to the BCA data storage memory 21 of BCA data. For this reason, the recording position of ECC parity becomes being the same as that of the time of the maximum data length of n= 12 also, for example by the case of n= 3.
[0065]The address generation of the data non-recording position at the time of the BCA reproduction to the addresses 48-191 is performed also by the case of n= 3, without flying. That is, the address generation at the time of the error correction processing by ECC parity will be performed as in the case of the maximum data length of n= 12 irrespective of the value of n.
[0066]thus, the reason for the ability to perform the processing same nevertheless as the time of n= 12 that is not n= 12, It is because it is not necessary to insert zero false data "00h" like before in order for zero data at the time of the memory initialization mentioned above "00h" to remain from EDC parity before ECC parity at the time of n!=12.
[0067]For this reason, the calculation result of the syndrome computed in the case of an ECC operation becomes completely the same as the syndrome calculation generated at the time of BCA data creation. By this, ECC processing may be unified irrespective of BCA record data length at the time of the maximum data length of n= 12.
[0068]Next, the address generation for EDC data processing also serves as the same processing as the time of the maximum record length of n= 12. That is, it **********s an address generation

one by one from 0, and is completed in 191, and an EDC parity position serves as the address (that is, zero data "00h" remains) 188,189,190,191 which is not recorded at the time of reproduction.
[0069]thus, the reason for the ability to perform the processing same nevertheless as the time of n= 12 that is not n= 12, For example, when the EDC result of an operation is generated from the address 0 to the address 47 which is a recording position of the 4th byte of actual EDC parity in the case of n= 3, it has become final and conclusive, At the time, if 0, i.e., an EDC check result, is O.K., the result of an operation, Even if it inputs zero data after it to the address 191, the EDC calculation result which performs EXCLUSIVE OR operation should be too set to 0, and it is because the EDC result of an operation previously settled in the address 47 will be held as it is. By this, EDC processing may be unified irrespective of BCA record data length at the time of the maximum data length of n= 12.
[0070]By initializing the contents of the BCA data storage memory 21 beforehand, and fixed-length-izing the data length, when data length records unspecified BCA data on the BCA data storage memory 21 according to the above-mentioned embodiment, Since ECC data processing and EDC data processing are unified into the processing at the time of the maximum data length and it enabled it to perform them irrespective of data length, Complicated processing which detects the recording length of BCA data is not needed like before, but it becomes possible to process BCA data easily with simple composition.
[0071]The above-mentioned BCA detector circuit 19 generates the identification information which shows whether the reproduced BCA data was recorded on the BCA data storage memory 21, and it may be made to record it on the BCA data storage memory 21. This invention is not limited to the above-mentioned embodiment, in the range which does not deviate from that gist in this outside, can change variously and can be carried out.
[0072]
[Effect of the Invention]As explained in full detail above, according to this invention, complicated processing which detects the recording length of BCA data is not needed, but the very good data reproduction apparatus which made it possible to process BCA data easily with simple composition can be provided.

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TECHNICAL FIELD

[Field of the Invention]This invention relates to improvement of the data reproduction apparatus which reproduces the data whose data length is un-specific.

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PRIOR ART

[Description of the Prior Art]As everyone knows, recently, DVD (Digital Video Disk) is developed as an optical disc which recorded a vast quantity of abbreviation 5G bit data on one side, and the DVD reproducer which plays this DVD is also spreading through a commercial scene.
[0003]By the way, after a manufacturing process is completed, for example at a factory etc. to this DVD, as shown in drawing 4, the so-called BCA (Burst Cutting Area) code may be further recorded on the specific region of inner circumference by the YAG laser rather than that read in area.
[0004]Drawing 5 shows the structure of one packet of such BCA data. The number of BCA user data has 16n-four (1<=n<=12) bytes' variable information area, and to this First, 4 bytes of EDC (Error Detection Code) parity, 16 bytes of ECC (Error Correction Code) parity is added.
[0005]And 1 byte of sync data RSBCAn are added to this variable information area and EDC parity every 4 bytes, respectively, and 1 byte of sync-data RSBCA13 is added to them every 4 bytes at ECC parity.
[0006]As for this BCA data, 1 byte of sync data SBBCA and 4 bytes of BCA-Preamble data whose each is "00h (Hexa-decimal)" are added to that head part.
[0007]After that ECC parity, 1 byte of sync-data RSBCA14 and 4 bytes of BCA-Postamble data whose each is "55h" are added, and, as for this BCA data, 1 byte of sync-data RSBCA15 is added after that.
[0008]And each sync data SBBCA and RSBCAn, RSBCA13, RSBCA14, and RSBCA15 comprise 8 channel bits which express a specific sink pattern, respectively, and 8 channel bits showing frame number n. 1 bit follows the modulation rule which becomes two channel bits.
[0009]Here, although the number of user data of one frame is formed at 16 bytes, only the n-th frame, the number of user data will be 12 bytes, and 4 bytes of EDC parity is added. For example, if it becomes n=5, the number of user data will be 16x5-4=76 byte, and 4 bytes of EDC parity will be added after sync-data RSBCAof five frames5 of the 4th line.
[0010]16 bytes of reed-solomon ECC parity which interleave processing is carried out and is added to the lengthwise direction of this BCA data structure belongs to 13 frames irrespective of user-datum length. For example, if it becomes n=5, sync-data RSBCA13 will appear after the EDC parity of five frames, and ECC parity will continue.
[0011]As mentioned above, rather than read in area of DVD, it has still more sufficient width on the concentric circle of inner circumference, and this BCA data is recorded, and its data non-record section in the BCA data recording regions on DVD increases, so that data length is short.
[0012]And the modulation rule of this BCA data is assigning two channel bits of "10" and "01" to the 1-bit data showing "0" and "1", respectively. A specific sink pattern is "01000110" from a higher rank, and the frame number following this is modulating the 4-bit data showing "0"- "13" to eight channel bits in accordance with the modulation rule mentioned above.
[0013]If this modulation rule is followed, the minimum polarity-reversals interval Tmin of data will be set to 1T, the maximum polarity-reversals interval Tmax will be set to 4T, and this 4T pattern will

appear only in sync data.
[0014]Drawing 6 shows the refreshable disk reproduction device for the optical disc in which such BCA data was recorded. In drawing 6, the numerals 11 are the optical discs in which BCA data was recorded, and are rotated with the disk motor 12. The signal recording surface of the optical disc 11 is countered, and the optical pick-up 13 is installed.
[0015]As for this disk motor 12, that revolving speed is controlled by the servo circuit 14. While a tracking servo and a focus servo are given, movement to the diameter direction of the optical disc 11 is controlled. [as opposed to / in the optical pick-up 13 / the object lens which is not illustrated by the servo circuit 14]
[0016]When playing the BCA data of the optical disc 11, control MPU(Micro-Processing Unit) 15 which controls operation of a disk reproduction device in generalization here, While giving a CAV (Constant Angular Velocity) servo by the servo circuit 14 so that the optical disc 11 may be kept at 24 Hz (1440 rpm) which is the optimal number of rotations for playback of BCA data, The optical pick-up 13 is moved to the record section of BCA data.
[0017]And after passing the amplifying circuit 16 and the equalizer circuit 17, the electrical signal corresponding to the BCA data outputted from the optical pick-up 13 is supplied to the data slicing circuit 18, and is binary-ized. This binary-ized signal is supplied to the BCA detector circuit 19 and the PLL (Phase Locked Loop) circuit 20.
[0018]Among these, PLL circuit 20 generates a channel bit clock from the inputted binary-ized signal, and is outputting it to the BCA detector circuit 19. From the inputted binary-ized signal, the BCA detector circuit 19 samples data based on a channel bit clock, and is generating the BCA detection channel bit.
[0019]And in this BCA detector circuit 19, the frame number has been obtained by detecting a sink pattern out of a BCA data stream, and restoring to the data of eight channel bits which continue after that based on a channel bit clock and a BCA detection channel bit.
[0020]Then, this BCA detector circuit 19 generates the row numbers in a frame from 0 to 3 to the obtained frame number, determines the address to the BCA data storage memory 21, and makes the BCA data to which it restored memorize one by one. 208 bytes is recorded, when this BCA data storage memory 21 is n= 12 when BCA data is the longest that is,.
[0021]As for the BCA data recorded on this BCA data storage memory 21, error detection based on [again] EDC parity in the error correction processing based on ECC parity is performed by the BCA data processing circuit 22.
[0022]Drawing 7 shows the details of the above-mentioned BCA detector circuit 19. That is, it is supplied to the sink detector circuit 19e while it is outputted to a data bus via the demodulator circuit 19b and the output terminal 19c, after the BCA binary-ized signal outputted from the above-mentioned data slicing circuit 18 passes the input terminal 19a. The channel bit clock outputted is supplied to the above-mentioned demodulator circuit 19b and the sink detector circuit 19e via the input terminal 19d from above-mentioned PLL circuit 20.
[0023]And the output of the above-mentioned demodulator circuit 19b and the output of the sink detector circuit 19e are outputted to the BCA data processing circuit 22 via 19h of BCA recording length detector circuits, and the output terminal 19i while they are outputted to an address bus via 19f of memory address generating circuits, and the output terminal 19g.
[0024]Here, if the above-mentioned optical pick-up 13 arrives at BCA data recording regions from the data non-record section of the optical disc 11, the channel bit which begins from the sync data SBBCA will be detected. Then, PLL circuit 20 locks and a regular channel bit clock comes to be obtained in the hit which reproduces these sync data SBBCA and BCA-Preamble data.
[0025]At this time, first, the sink pattern of sync-data RSBCA1 is detected and the address 0 is generated in the BCA data storage memory 21 in the above-mentioned BCA detector circuit 19. Then, the BCA detector circuit 19 performs data demodulation processing which is detected and which makes it 1 byte every 16 channel bits, and is **********ing the address each time.

[0026]Thus, when the data for 4 bytes was recorded on the BCA data storage memory 21 next, sync-data RSBCA1 should be detected again, but. Even if undetectable, it continues without changing a data demodulation interval and increment of an address as what has detected sync data in false, and the BCA detector circuit 19 is performing what is called synchronous protection.
[0027]If the BCA detector circuit 19 sets up the sink detection window about **2 channel-bit width and sync data are detectable in this window to the predicted position which detects sync data, it will perform that position amendment and will correct subsequent data demodulation synchronizations.
[0028]When the sync data detected at this time are the values of RSBCA10 other than RSBCA1 (for example, RSBCA2), etc., the BCA detector circuit 19 considers that it is a detection error, and is kept from changing an address.
[0029]And when the demodulated data for 16 bytes is recorded on the BCA data storage memory 21, the sync data by which it is generated next must be RSBCA2 or RSBCA13, but. The BCA detector circuit 19 is not based on a frame number, but makes increment of an address continue, and is made to continue without also changing a data demodulation synchronization.
[0030]That is, even if there is a change data demodulation synchronous [by position amendment of **2 channel bit by sync data], increment is continued about an address. Thus, the address to each byte of the user datum, its EDC parity, and ECC parity at the time of generating an address will be generated as shown in drawing 8.
[0031]A recovery and record of data are performed by the above procedure, and recording operation is ended when 16 bytes of data in which sync-data RSBCA13 was added is recorded. Next, processing of an error correction, EDC error detection, etc. is performed to the data recorded on the above-mentioned BCA data storage memory 21 by the BCA data processing circuit 22. That is, in the above-mentioned BCA detector circuit 19, when recording BCA data on the BCA data storage memory 21, the recording address of final data (RSBCA13) was held and this address is sent out to the BCA data processing circuit 22.
[0032]In this BCA data processing circuit 22, first, although error correction processing by ECC parity is performed, ECC parity is generated by the syndrome calculation by the data permutation of a lengthwise direction here. Therefore, in this error correction processing, it is made to advance an address to a lengthwise direction by four rows.
[0033]Namely, since the ECC parity to which the data which is 16 bytes to which sync-data RSBCA3 was given per 4 bytes, next sync-data RSBCA13 were given continues in being n= 3, for example, From 0 to 15 becomes data of RSBCA1, from 16 to 31 becomes data of RSBCA2, from 32 to 47 becomes data of RSBCA3, and, as for an address, even 63 becomes the ECC parity of RSBCA13 from 48.
[0034]For this reason, the address generated for the error correction of the 1st row is 0->4->8->12->.... It is set to ->56 ->60 and ECC parity will exist in the position of the addresses 48, 52, 56, and 60. At the time of the error correction of the 2nd row, it is an address 1->5->9->13-> .... It is made to generate with ->57 ->61 and the addresses 49, 53, 57, and 61 serve as a position of ECC parity in this case.
[0035]Similarly, at the time of the error correction of the 3rd row, it is an address 2->6->10->14-> .... It is made to generate with ->58 ->62, In this case, the addresses 50, 54, 58, and 62 serve as a position of ECC parity, and it is an address at the time of the error correction of the 4th row 3->7->11->15-> .... It is made to generate with ->59 ->63 and the addresses 51, 55, 59, and 63 serve as a position of ECC parity in this case.
[0036]By the way, ECC parity is made from the format of the BCA code corresponding to the time of the maximum record length of a BCA user datum, i.e., the case of n= 12. For this reason, in the case of n!=12, zero data "00h" must be put into the crevice from EDC parity to ECC parity, and syndrome calculation must be performed.
[0037]For this reason, it is necessary to insert zero data "00h" in this crevice virtually, and to

perform syndrome calculation also in the case of error correction processing of BCA data. If it says in the above-mentioned example (n= 3), in the case of the error correction of the 1st row. x (12-3) 4= 36 bytes of zero data "00h" needs to be inserted as a crevice at the time of the maximum record length between the address 44 in which EDC parity is located, and the address 48 in which the 1st byte of ECC parity is located.

[0038]And in the above-mentioned BCA data processing circuit 22. A crevice is calculated from the recording address of the recording length detected in 19 h of BCA recording length detector circuits of the BCA detector circuit 19, i.e., the data of sync-data RSBCA13 obtained by the above-mentioned record method, and zero dummy data "00h" is inserted.

[0039]That is, if it is n= 6, as for the 1st row, an address is 0->4->8->12->.... Since it is generated with ->104 ->108 and the address 96,100,104,108 serves as ECC parity in this case, Among the addresses 92 and 96, x (12-6) 4= 24 bytes of zero data "00h" will be inserted.

[0040]Next, data processing for the EDC error detection in the above-mentioned BCA data processing circuit 22 is explained. That is, he is trying to double processing with recording length using the recording address of the final data held at the time of data recording at the time of this EDC data processing as well as the time of ECC processing.

[0041]For example, if it is n= 3, the address generated will be 0 to 63 and the address of EDC parity will become 44, 45, 46, and 47 before long. For this reason, the address generated at the time of EDC data processing begins from 0, and is ended by 47. If it is n= 6, the address generated will be 0 to 111 and the address of EDC parity will become 92, 93, 94, and 95 before long. For this reason, the address generated at the time of EDC data processing begins from 0, and is ended by 95.

[0042]As mentioned above, BCA data in a refreshable disk reproduction device. For the error correction by ECC parity, or EDC check processing, supply the recording length whom the BCA detector circuit 19 detected to the BCA data processing circuit 22, and in the BCA data processing circuit 22. According to this inputted detection recording length, he chooses ECC-error-correction processing or EDC data processing, and is trying to change processing.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention]As explained in full detail above, according to this invention, complicated processing which detects the recording length of BCA data is not needed, but the very good data reproduction apparatus which made it possible to process BCA data easily with simple composition can be provided.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, in the above conventional disk reproduction devices. Since it has changed so that the recording length of BCA data may be detected and processing of ECC and EDC may be made to correspond according to this recording length that detected, the problem of the processing which BCA data reproduction takes being complicated, and circuitry being also complicated and enlarging it according to this has arisen.
[0044]Then, this invention was made in consideration of the above-mentioned situation, and does not need complicated processing which detects the recording length of BCA data, but it aims at providing the very good data reproduction apparatus which made it possible to process BCA data easily with simple composition.

[Translation done.]

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MEANS

[Means for Solving the Problem]One data packet comprises a frame of an unspecified number, and a data reproduction apparatus concerning this invention is aimed at what reproduces a data row which comprises data of a predetermined number to which a synchronization code and a frame number were given, respectively by one frame.
[0046]And a recording medium which has the storage capacity which can record one data packet in which a frame of the maximum number was contained, An initializing means which records and initializes specific data to a record section for one data packet of this recording medium, An address given to a recording medium from a synchronization code and a frame number which are contained in a reproduced data packet is generated, and it has a recording device which records data of a data packet reproduced based on this generated address on a recording medium.
[0047]When a frame number records an unspecified data row on a recording medium according to the above composition, Record specific data on a recording medium, initialize the contents, and an address given to a recording medium from a synchronization code and a frame number which are contained in a data packet reproduced on it is generated, Itis [fixed-length-] made toize data length by recording data of a data packet reproduced based on this generated address on a recording medium.
[0048]For this reason, as opposed to data of a data packet recorded on a recording medium irrespective of data length, can unify ECC data processing, EDC data processing, etc. into processing at the time of the maximum data length, can perform them now, and like before, It becomes possible to process a data row easily with simple composition, without needing complicated processing which detects recording length of BCA data.
[0049]
[Embodiment of the Invention]Hereafter, this embodiment of the invention is described in detail with reference to drawings. In drawing 1, identical codes are attached and shown in drawing 6 and identical parts. That is, it does not carry out detecting the recording length of BCA data in said BCA detector circuit 19, but the line which sends out recording length to the BCA data processing circuit 22 is deleted from the BCA detector circuit 19. And it has composition as shows drawing 2 the BCA detector circuit 19. In drawing 2, identical codes are attached and shown in drawing 7 and identical parts.
[0050]Here, said BCA data storage memory 21 has the capacity which can memorize 208 bytes which is a data number in case BCA data is the longest, i.e., n= 12. And in detecting BCA data, said control MPU15 generates memory initialization instructions via the input terminal 19j in the memory initialization control circuit 19k of the BCA detector circuit 19.
[0051]In response to these memory initialization instructions, the BCA detector circuit 19, To the BCA data storage memory 21, as shown in drawing 3, "FFh" is written in the addresses 0-15 as un-0 data, Memory initialization processing in which write zero data "00h" in the addresses 16-191, and "FFh" is written in the addresses 192-207 as un-0 data is performed.

[0052]This memory initialization processing by decoding the address generated in 19 f of memory address generating circuits by 19 l. of address decoders, By the addresses 0-15, and 192-207, so that un-0 data "FFh" may be generated from the output terminal 19c, The control signal A ("H"active) is outputted to 19 m of OR circuits, and in other addresses (16-191 are included), the control signal B ("L"active) is outputted to 19 n of AND circuits so that zero data "00h" may be generated from the output terminal 19c.
[0053]And when this memory initialization processing is completed, the BCA detector circuit 19 starts the detecting operation of BCA data. That is, control MPU15 generates instructions so that the optical pick-up 13 may be moved to the record section of BCA data, while making a CAV servo perform to the servo circuit 14 so that the optical disc 11 may be maintained at the optimal number of rotations for playback of BCA data.
[0054]Here, if the above-mentioned optical pick-up 13 arrives at BCA data recording regions from the data non-record section of the optical disc 11, the channel bit which begins from the sync data SBBCA will be detected. Then, PLL circuit 20 locks and a regular channel bit clock comes to be obtained in the hit which reproduces these sync data SBBCA and BCA-Preamble data.
[0055]At this time, first, the sink pattern of sync-data RSBCA1 is detected and the address 0 is generated in the BCA data storage memory 21 in the above-mentioned BCA detector circuit 19. Then, the BCA detector circuit 19 performs data demodulation processing which is detected and which makes it 1 byte every 16 channel bits, and is **********ing the address each time.
[0056]Thus, when the data for 4 bytes was recorded on the BCA data storage memory 21 next, sync-data RSBCA1 should be detected again, but. Even if undetectable, it continues without changing a data demodulation interval and increment of an address as what has detected sync data in false, and the BCA detector circuit 19 is performing what is called synchronous protection.
[0057]If the BCA detector circuit 19 sets up the sink detection window about **2 channel-bit width and sync data are detectable in this window to the predicted position which detects sync data, it will perform that position amendment and will correct subsequent data demodulation synchronizations.
[0058]When the sync data detected at this time are the values of RSBCA10 other than RSBCA1 (for example, RSBCA2), etc., the BCA detector circuit 19 considers that it is a detection error, and is kept from changing an address.
[0059]And when the demodulated data for 16 bytes is recorded on the BCA data storage memory 21, the sync data by which it is generated next must be RSBCA2 or RSBCA13, but if the detected frame number is except 13, an address will continue increment, without changing.
[0060]When the sink pattern of sync-data RSBCA13 is detected in the window of **2 channel-bit width to a predicted position, 19 f of memory address generating circuits output the address 192 (address jump). Since this address 192 is equivalent to the address which writes in the 1st byte of RSBCA13 at the time of the maximum record length, zero data "00h" written in at the time of memory initialization will remain in the jumped addresses 16-191 after all. And recording operation is ended when 16 bytes of data in which sync-data RSBCA13 was added is recorded.
[0061]Next, processing of an error correction, EDC error detection, etc. is performed to the data recorded on the BCA data storage memory 21 as mentioned above by the BCA data processing circuit 22. First, address generation for the error correction processing by ECC parity is performed as follows.
[0062]That is, the address generated for error correction processing of the 1st row is 0->4->8->12->.... It is set to ->200 ->204 and ECC parity will exist in the position of the address 192,196,200,204. The address generated for error correction processing of the 2nd row is 1->5->9->13->.... It is set to ->201 ->205 and ECC parity will exist in the position of the address 193,197,201,205.
[0063]Similarly, the address generated for error correction processing of the 3rd row is 2->6->10->14->.... It is set to ->202 ->206 and ECC parity will exist in the position of the address

194,198,202,206. The address generated for error correction processing of the 4th row is 3->7->11->15->.... It is set to ->203 ->207 and ECC parity will exist in the position of the address 195,199,203,207.

[0064]And the ECC parity following sync-data RSBCA13 is recorded on the fixed position 192-207 of the memory 21, i.e., addresses, at the time of record to the BCA data storage memory 21 of BCA data. For this reason, the recording position of ECC parity becomes being the same as that of the time of the maximum data length of n= 12 also, for example by the case of n= 3.

[0065]The address generation of the data non-recording position at the time of the BCA reproduction to the addresses 48-191 is performed also by the case of n= 3, without flying. That is, the address generation at the time of the error correction processing by ECC parity will be performed as in the case of the maximum data length of n= 12 irrespective of the value of n.

[0066]thus, the reason for the ability to perform the processing same nevertheless as the time of n= 12 that is not n= 12, It is because it is not necessary to insert zero false data "00h" like before in order for zero data at the time of the memory initialization mentioned above "00h" to remain from EDC parity before ECC parity at the time of n!=12.

[0067]For this reason, the calculation result of the syndrome computed in the case of an ECC operation becomes completely the same as the syndrome calculation generated at the time of BCA data creation. By this, ECC processing may be unified irrespective of BCA record data length at the time of the maximum data length of n= 12.

[0068]Next, the address generation for EDC data processing also serves as the same processing as the time of the maximum record length of n= 12. That is, it **********s an address generation one by one from 0, and is completed in 191, and an EDC parity position serves as the address (that is, zero data "00h" remains) 188,189,190,191 which is not recorded at the time of reproduction.

[0069]thus, the reason for the ability to perform the processing same nevertheless as the time of n= 12 that is not n= 12, For example, when the EDC result of an operation is generated from the address 0 to the address 47 which is a recording position of the 4th byte of actual EDC parity in the case of n= 3, it has become final and conclusive, At the time, if 0, i.e., an EDC check result, is O.K., the result of an operation, Even if it inputs zero data after it to the address 191, the EDC calculation result which performs EXCLUSIVE OR operation should be too set to 0, and it is because the EDC result of an operation previously settled in the address 47 will be held as it is. By this, EDC processing may be unified irrespective of BCA record data length at the time of the maximum data length of n= 12.

[0070]By initializing the contents of the BCA data storage memory 21 beforehand, and fixed-length-izing the data length, when data length records unspecified BCA data on the BCA data storage memory 21 according to the above-mentioned embodiment, Since ECC data processing and EDC data processing are unified into the processing at the time of the maximum data length and it enabled it to perform them irrespective of data length, Complicated processing which detects the recording length of BCA data is not needed like before, but it becomes possible to process BCA data easily with simple composition.

[0071]The above-mentioned BCA detector circuit 19 generates the identification information which shows whether the reproduced BCA data was recorded on the BCA data storage memory 21, and it may be made to record it on the BCA data storage memory 21. This invention is not limited to the above-mentioned embodiment, in the range which does not deviate from that gist in this outside, can change variously and can be carried out.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]The block lineblock diagram showing the embodiment of the data reproduction apparatus concerning this invention.
[Drawing 2]The block lineblock diagram showing the details of the important section in the embodiment.
[Drawing 3]The figure shown in order to explain the memory initialization processing in the embodiment.
[Drawing 4]The top view shown in order to explain the record section of the BCA data on an optical disc.
[Drawing 5]The figure shown in order to explain the format of the BCA data.
[Drawing 6]The block lineblock diagram showing the conventional disk reproduction device which reproduces the BCA data.
[Drawing 7]The block lineblock diagram showing the details of the important section in the disk reproduction device.
[Drawing 8]The figure showing the example of generation of the address in the disk reproduction device.
[Description of Notations]
11 -- Optical disc
12 -- Disk motor,
13 -- Optical pick-up
14 -- Servo circuit
15 -- Control MPU,
16 -- Amplifying circuit,
17 -- Equalizer circuit
18 -- Data slicing circuit
19 -- BCA detector circuit,
20 -- PLL circuit
21 -- BCA data storage memory,
22 -- BCA data processing circuit.

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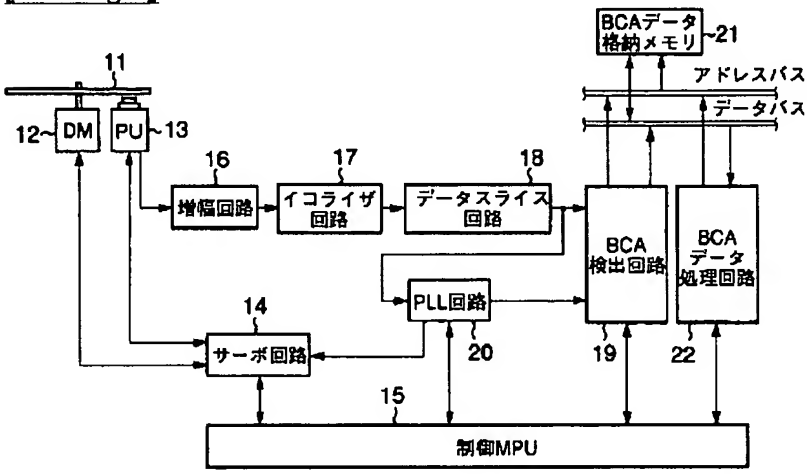
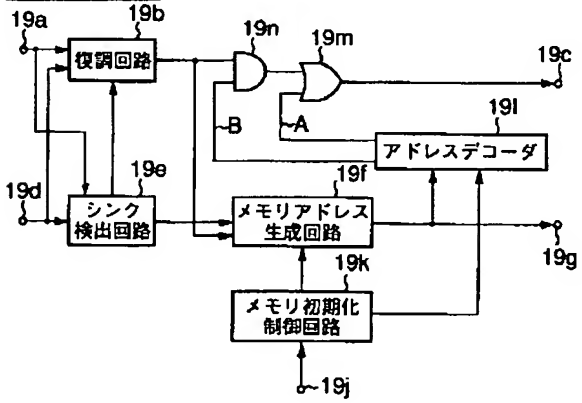
DRAWINGS

[Drawing 1]



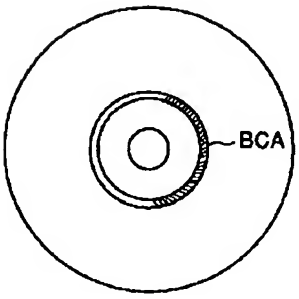
[Drawing 2]



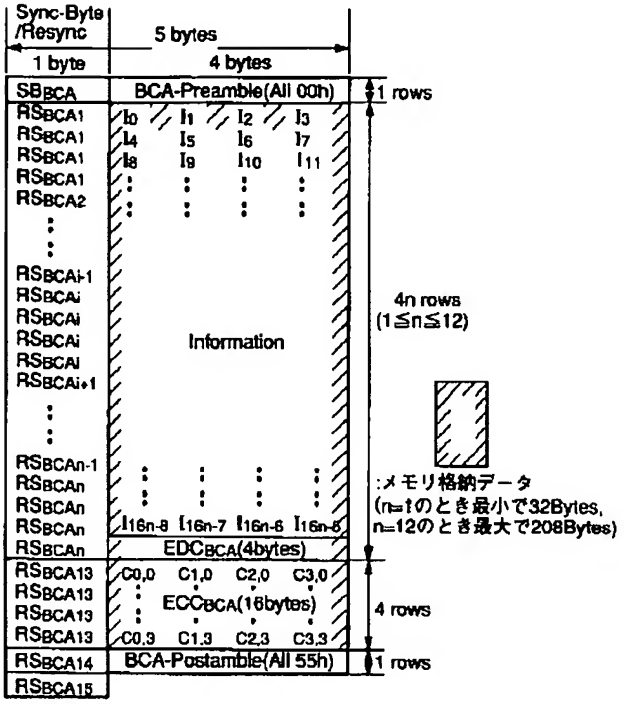
[Drawing 3]

FFh	FFh	FFh	FFh	
FFh	FFh	FFh	FFh	
FFh	FFh	FFh	FFh	
FFh	FFh	FFh	FFh	
00h	00h	00h	00h	
00h	00h	00h	00h	
00h	00h	00h	00h	
00h	00h	00h	00h	
00h	00h	00h	00h	
00h	00h	00h	00h	
⋮	⋮	⋮	⋮	48 rows
⋮	⋮	⋮	⋮	
00h	00h	00h	00h	
00h	00h	00h	00h	
00h	00h	00h	00h	
00h	00h	00h	00h	
FFh	FFh	FFh	FFh	
FFh	FFh	FFh	FFh	4 rows
FFh	FFh	FFh	FFh	
FFh	FFh	FFh	FFh	

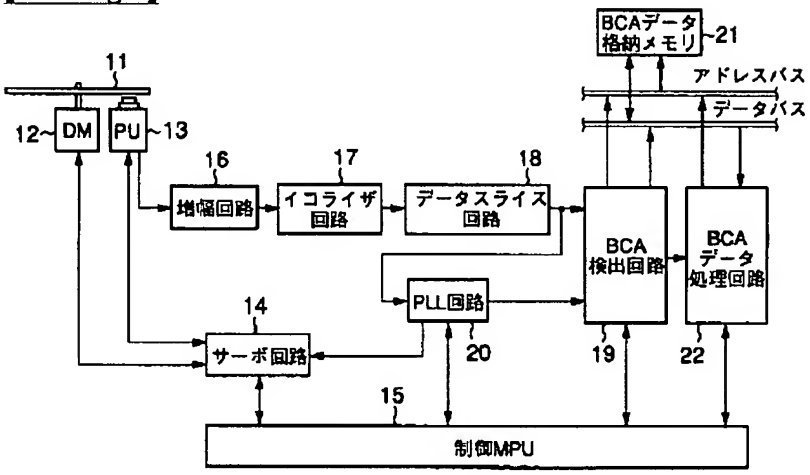
[Drawing 4]



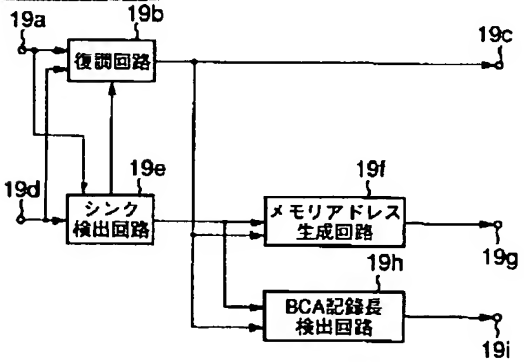
[Drawing 5]



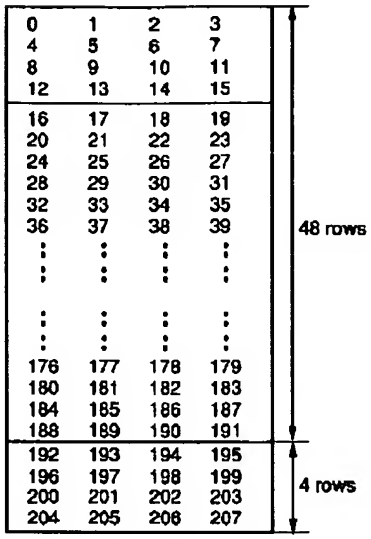
[Drawing 6]



[Drawing 7]



[Drawing 8]



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